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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,757	02/14/2002	Claude Gauthier	03226.171001;P7189	9460

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EXAMINER	
JONES, HUGH M	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,757	GAUTHIER ET AL.	
	Examiner	Art Unit	
	Hugh Jones	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/14/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 of U. S. Application 10/075,757, filed February 14, 2002, are pending.

Claim Interpretation

2. The following interpretations were taken in order to examine the claims. The 'simulation' is a simulation carried out on a computer. The 'representative power supply waveform' is the waveform as required by the digital simulation and thus is characterized by amplitude, rise time, fall time and duration. The 'representative power supply waveform' is not an actual measured waveform, because it is unclear how such a waveform could be entered into the digital simulation. It is further interpreted that art teaching simulation of the PLL for use in a chip applies equally well to a chip package as well as a printed circuit board. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Furthermore, Applicant's admissions regarding knowledge of those skilled in the art are noted – see paragraphs 31-36, for example, of the specification.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,819,192 in view of Heydari et al..

7. The patented claims appear to recite the same features but do not appear to recite adjusting an amount of decoupling capacitance. Heydari et al. disclose the effect of decoupling capacitance on PLL jitter. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the patented claimed features with the Heydari et al. teachings because Heydari et al. disclose (col. 1, page 444, top) that on-chip switching noise can be effectively eliminated via use of decoupling capacitors.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1, 4-5, 7, 9-12, 15-16, 18, 20-23, 26-27, 29, 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heydari et al.

11. Heydari et al. disclose the effect of decoupling capacitance on PLL jitter and power supply noise (Fig. 2) for a chip and a comparison of simulated with measured data (section VI). See also section V (PLL jitter analysis).

12. The section on the simulation doesn't expressly disclose that values of the decoupling capacitance are iterated during the simulation.

13. Fig. 2 shows the effects of differing values of the decoupling capacitors on power supply noise.

14. It would have been obvious to one of ordinary skill in the art at the time of the invention to iterate the values of the decoupling capacitors during the simulation as disclosed in section VI, because fig. 2 shows the effects of differing values of decoupling capacitance on power supply noise and the abstract discloses that power supply noise translates into jitter. Furthermore, col. 1, page 444, top discloses that on-chip switching noise can be effectively eliminated via use of decoupling capacitors.

15. Claims 2-3, 6, 8, 13-14, 17, 19, 24-25, 28, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heydari et al. in view of Applicant's Own Admission.

16. Heydari et al. disclose the intervening limitations as discussed.

17. Heydari et al. do not expressly disclose some of the details as recited in the dependent claims, such as where the power supply waveform is obtained.

18. Applicants have admitted (paragraphs 31-36) the knowledge of those skilled in the art, including sources for power supply waveforms, probing for the waveforms, sources for noise, and the dependence of noise on various parameters; that the simulations of the power supply and the PLL can be from different simulators; that the waveform can be obtained from a location adjacent to the intended location of the PLL.

Response to Arguments

19. Applicant's arguments filed 12/27/2005 have been fully considered but they are not persuasive. Applicants are thanked for their response.

20. Applicant's arguments regarding the double patenting rejections are not persuasive. Applicants appear to be mixing the issues of double patenting and prior art rejections. Applicants have not cited any case law or section of the MPEP in support. Applicants have made no other argument.

21. Applicant's arguments relating to the prior art rejections on page 2 to the top of page 5 are not persuasive. Please see fig. 2 which discloses results of a *simulation* (see text relating to fig. 2) of the *effects of decoupling capacitance*. Note the sentence in the section (which discusses the simulation) above the figure:

"If the decoupling capacitance is made much larger than the switched capacitances, then the on-chip switching noise can be effectively eliminated."

Thus, other *continuous* values of the decoupling capacitance were simulated than the two discrete values as Applicants argue. But, even assuming Applicant's premise, there would have still been motivation to simulate other values, as asserted in paragraph 14 of the office action. Applicants have not addressed said motivation in paragraph 14.

22. Applicants further appear to suggest that the "mathematical model" in Heydari is not a simulation. This is not persuasive.

23. Applicants also appear to argue that the simulation disclosed in Heydari is to be used for another purpose than the simulation recited in the claims. Heydari clearly discloses the effects of decoupling capacitance on PLL circuits in a simulation of such circuits; the claims recite changing the decoupling capacitance of a PLL circuit because of the effects of the capacitance. But, even hypothetically assuming Applicant's premise, the fact that applicant may have recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

24. Furthermore, in response to applicant's arguments, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from

the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

25. Paragraphs 31-36 are recited (emphasis added) clearly indicate that those skilled in the art were well aware of noise in circuits and how to simulate their effects:

"[0031] Those skilled in the art will appreciate that the captured power supply waveform having noise may be obtained from probing a physical system, such as a printed circuit board, chip package, or chip, under various operating conditions. Operating conditions include, but are not limited to, temperature, voltage, frequency, and manufacturing (process) variations. Those skilled in the art will also appreciate that the captured power supply waveform having noise may be obtained from probing an integrated circuit under various operating conditions. Furthermore, those skilled in the art will appreciate that the power supply waveform having noise obtained from a physical system may be obtained from a location adjacent to an intended location of the PLL under various operating conditions. Those skilled in the art will further appreciate that using the power supply waveform having noise in place of a portion of the power supply network reduces the computational load when simulating the circuit.

[0032] Those skilled in the art will appreciate that the captured power supply signal having noise may be obtained from simulation data of a modeled printed circuit board's parasitics under various operating conditions. Furthermore, those skilled in the art will appreciate that the captured power supply waveform having noise may be obtained from simulation data of a power supply network's parasitics that may include, but is not limited to, the motherboard power supply network, motherboard to integrated circuit connections, and/or integrated circuit power supply network under various operating conditions. Operating conditions include, but are not limited to, temperature, voltage, frequency, and manufacturing (process) variations. Those skilled in the art will further appreciate that the simulation of the circuit using the power supply waveform having noise may be dependent on various operating conditions. Those skilled in the art will also appreciate that the simulation tool used to capture the power supply waveform having noise does not have to be the same simulation tool used to simulate the circuit using the power supply waveform having noise.

[0033] Those skilled in the art will appreciate that capturing the power supply signal having noise, whether from a physical system or simulation, may advantageously be obtained adjacent to an intended location of the PLL.

[0034] Those skilled in the art will appreciate that the noise may be captured separately from the power supply waveform and combined to create the power supply waveform having noise.

[0035] Those skilled in the art will appreciate that multiple power supply waveforms having noise may be used simultaneously, and the multiple power supply waveforms having noise may be connected to different locations on the power supply network. Those skilled in the art will further appreciate that the PLL and additional circuits may be used in the simulation at (178).

[0036] Those skilled in the art will appreciate that the PLL may be analog, digital, or a combination of both types of circuits."

Conclusion

26. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (571) 272-3781,

Monday-Thursday 0830 to 0700 ET,

or

the examiner's supervisor, Kamini Shah, telephone number (571) 272-2279.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or (703) 308-1396 (for informal or draft communications, please label *PROPOSED* or *DRAFT*).

Dr. Hugh Jones

Primary Patent Examiner

March 11, 2006